Printed Silver Grid Incorporated With PEIE Doped ZnO as an Auxiliary Layer for High-Efficiency Large-Area Sprayed Organic Photovoltaics

Yu-Ching Huang, De-Han Lu, Chia-Feng Li, Cheng-Wei Chou, Hou-Chin Cha, and Cheng-Si Tsao

***Abstract*—The aim of this study is to mitigate the loss of performance of organic photovoltaics when the device area is increased. We propose that performance reduction is a result of the poor transverse charge transport due to defects in the electron transport layer and the resistance of the transparent electrode. We modified the surface of a zinc oxide (ZnO) with ethoxylated polyethylenimine and successfully lowered the performance reduction from 30% to 15% based on two electron transport layers of ZnO and ethoxylated polyethylenimine (PEIE)-modified ZnO (ZnO/PEIE bilayer and ZnO:PEIE hybrid layer). We also deposited Ag grids on the indium-tin-oxide (ITO) substrate to facilitate transverse charge transport in the ITO.**

***Index Terms*—Large-area, module, organic photovoltaics (OPVs), silver grid, spray coating, surface modification.**

I. Introduction

SOLUTION-BASED organic photovoltaics (OPVs), as the next generation of photovoltaics, are an emerging technology with promising characteristics of easy-fabrication, flexibility, low-cost, low-carbon emission, thin-film structure, and light weight [1], [2]. Recently, the power conversion efficiency (PCE) of OPVs has been greatly improved to over 14% [3]–[5]. Such high PCE values have allowed OPVs to attract attention for their potential use in real applications. Therefore, developing large-area fabrication techniques and module designs for OPVs are critical for mass production and commercialization. Strip-shape OPVs with a width of 1 cm and a length of >8 cm are usually adopted as the unit cell of commercial modules via series connection [6], [7]. However, the scaling up of OPVs into such a unit cell generally causes a reduction in PCE compared to that of small-area OPVs (<0.3 cm^2) [8]. To date, how to fabricate long-strip OPVs with a minimal reduction in PCE remains an important issue but has not been sufficiently investigated. Several complex factors, including the bulk characteristics of various layers and the interfaces between layers in the cells, can hinder the transportation of charge carriers along the invisible paths or network in the large three-dimensional (3-D) space. This study demonstrates a simple approach based on the rational design of an inkjet-printed (IJP) silver grid to effectively solve this problem.

Recently, spray-coated OPVs have presented remarkable progress in performance [9]–[11], which proves that the spray process is a well-established process for large-area OPVs and module manufacturing. However, most studies mainly focus on processing small-area devices (<1 cm^2) instead of large-area devices. Good film uniformity and a low number of defects are important issues in large-area sprayed devices, but these issues have not been broadly studied in the research field yet. Previous literature has reported that reducing the resistive loss of ITO can be achieved by introducing metal subelectrodes, and thus, the PCE of large-area devices can be improved using a spin- or spray-coating process [12], [13]. However, the subelectrodes reported previously in the literature were deposited by thermal evaporation, which is not ideal for future mass production. It has been demonstrated that the combination of an inkjet-printed silver grid and a highly conductive polymer, such as poly(3,4-ethylenedioxythiophene):poly(styrenesulfonate), can effectively serve as an alternative transparent electrode to the commonly used indium tin oxide (ITO) [14]–[17]. In this study, we examined the possibility of utilizing an inkjet-printed silver grid as an auxiliary electrode to reduce the resistive loss of ITO, and thus improve the PCE of large-area sprayed OPVs. To maintain high-performance and good durability as the first requirement of the strip unit cell with 1×8 cm^2 active area, this work adopted an inverted architecture with a conventionally ITO-coated substrate [14], [18]. A blend of the commonly used poly(3-hexylthiophene) (P3HT) and [6,6]-phenyl-C_{61}-butyric acid methyl ester (PCBM) was used as the photoactive layer. ITO-coated glass substrates with different sheet resistances were adopted here. We focused on the problem of how to effectively collect the charge carriers transported along 3-D directions and reduce the adverse effects caused by coating inhomogeneities and material defects when the deposition processes of all layers are fixed. This study demonstrates the optimum design and improvement of performance tuned by a simple inkjet-printed Ag grid on the ITO substrate and modification of the electron transport layer (ETL). Nondestructive characterization was

Manuscript received April 5, 2019; revised May 15, 2019; accepted June 18, 2019. Date of publication July 12, 2019; date of current version August 22, 2019. This work was supported by the Ministry of Science and Technology of Taiwan under Grant 107-2218-E-131-007-MY3. *(Corresponding authors: Yu-Ching Huang; Cheng-Si Tsao.)*

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Digital Object Identifier 10.1109/JPHOTOV.2019.2925552

performed to validate the improved performance and correlate the performance with the modified structure.

II. Experimental Details

P3HT and PCBM were purchased from Rieke metals and Nano-C, respectively. A mixture of P3HT and PCBM (mass ratio = 1:1) dissolved in o-xylene with a concentration of 10 mg/mL was prepared to deposit active layer. ITO-coated glass was used as the cathode, and it exhibited a sheet resistance of 15 Ω/square. Before the ETL deposition, these ITO-coated substrates were ultrasonically cleaned with acetone and isopropanol, and then treated with nitrogen plasma. Zinc oxide (ZnO) was used as an ETL in the OPVs. Ethoxylated polyethylenimine (PEIE) was used to prepare a ZnO/PEIE bilayer and ZnO:$PEIE_{10}$ hybrid layer to improve the conductivity, film quality, and interface contact with the active layer. The materials and solutions prepared for both ZnO, PEIE, and ZnO:PEIE hybrid ETLs were described in a previous study [19]. PEIE was diluted in 2-methoxyethanol into a 0.4 wt% solution, and then diluted with IPA in the volume ratio of 1:18. For the ZnO/PEIE ETL, PEIE layer was spin-coated on the ZnO layer. As for the ZnO:PEIE hybrid ETL, ZnO precursor was mixed with a 10 vol% PEIE solution, and we named the ETL as ZnO:$PEIE_{10}$. All the ETLs and P3HT:PCBM active layers were spray-coated in ambient conditions using an ExactCoat system equipped with an AccuMist 120 kHz ultrasonic atomizing nozzle [15], [20]. The spray-coated ETLs were dried at 150 °C for 1 h. The spray-coated active layers were thermally annealed at 130 °C for 10 min in the ambient environment. Finally, the thermally evaporated MoO_3/Ag anode was deposited on the active layer. The reference OPV was fabricated with an inverted architecture: ITO-coated glass/ETL/active layer/MoO_3/Ag. The area of the strip cell devices was defined by the area of the MoO_3/Ag anode. The typical area was 1×8 cm^2. Some devices have a fixed width of 1 cm and different lengths of 1, 2, and 4 cm, respectively, for investigating the effect of the length.

In contrast to the reference OPV device, a simple Ag grid and a bus-bar connecting the grids for current collection were inkjet-printed onto the ITO-coated substrate prior to the deposition of the ETL. The subsequent processing steps of the investigated OPVs were the same as those of the reference OPV device. A schematic illustration of the OPV device with a simple current-collecting Ag grid investigated here is shown in Fig. 1. The curing temperature and time of the inkjet-printed Ag grids were 150 °C and 20 min, respectively. The width and thickness of Ag grids are 1 mm and ∼500 nm, respectively. Current–voltage (J–V) characteristics were measured by using a solar simulator (Abet technologies, Model #11000) under A.M. 1.5 illumination (100 mW/cm^2) and ambient conditions. Nondestructive characterization via 2-D EQE mapping of a strip OPV device was conducted by laser beam-induced current (LBIC).

III. Result and Discussion

A. Effect of PEIE Doped ZnO on the Performance Reduction of Large-Area Sprayed Organic Photovoltaics

Our previous study pointed out that a slot-die-coated ETL comprising ZnO nanoparticles has inherent defects that are unfavorable to charge collection [19]. The PEIE-modified ETL can improve the interface contact between the active layer and this modified ETL and reduce the defect traps throughout the bulk ETL, enhancing charge collection mainly along the vertical direction (normal to the substrate) and thus improving the PCE [19]. The J–V curves and performance of the spray-coated strip OPVs with ZnO, ZnO/PEIE, and ZnO:$PEIE_{10}$ ETLs as a function of length (the strip width is 1 cm) are shown in Fig. 2 and listed in Table I. Compared to the reference OPVs (device area = 1×0.3 cm^2), the devices based on PEIE-modified ETL exhibited ∼10% improvement in PCE. This improvement resulted from the increase in short-circuit current (J_{sc}) of ∼1 mA/cm^2. The increasing J_{sc} may be attributed to the improved vertical transport of charge carriers due to the modification by PEIE. Fig. 2(d) shows the reduction in PCE with increasing strip area; the PEIE-modified ETL can effectively improve the PCE reduction by 15% as compared with the devices with pristine ZnO ETLs. Decreases in the fill factor (FF) and PCE with

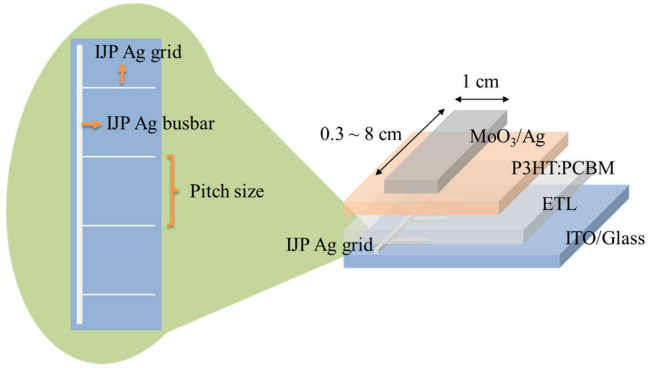

Fig. 1. Schemaitc illustration of the inverted OPVs with strip area of 1×0.3, 1×1, 1×2, 1×4 and 1×8 cm^2. The left-side strip OPV has the embedded inkjet-printed Ag grid lines. The other is the reference OPV. The geometry of the Ag grid and busbar is shown in the inset.

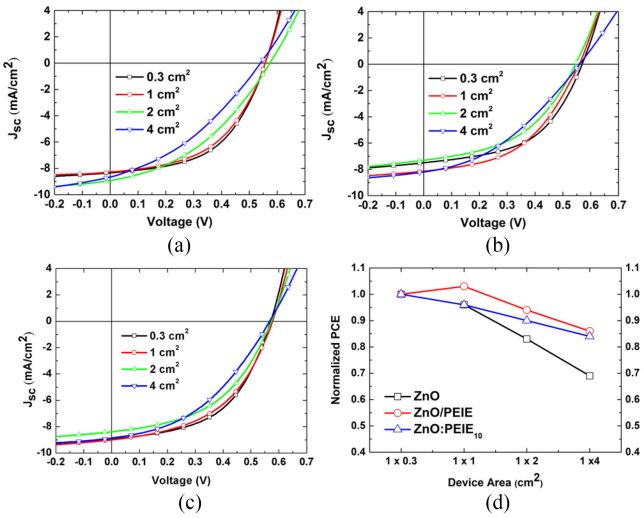

Fig. 2. Current–voltage behavior of spray-coated 1×0.3, 1×1, 1×2, and 1×4 cm^2 OPVs based on various ETL. (a) ZnO. (b) ZnO/PEIE. (c) ZnO:$PEIE_{10}$. (d) Reduction in PCE with increasing strip area.

TABLE I
PERFORMANCE OF SPRAY-COATED 1 × 0.3, 1 × 1, 1 × 2 AND 1 × 4 cm^2 OPVS WITH VARIOUS ETLS OF ZNO, ZNO/PEIE, AND ZNO:$PEIE_{10}$

ETL	Device Area (cm^2)	J_{sc} (mA cm^{-2})	V_{oc} (V)	FF	PCE (%)
ZnO	0.3	8.35	0.56	51.8	2.42
	1	8.29	0.56	49.9	2.31
	2	8.94	0.57	39.5	2.01
	4	8.69	0.54	35.7	1.68
ZnO/PEIE	0.3	9.27	0.58	50.6	2.72
	1	9.36	0.59	50.7	2.80
	2	9.22	0.58	48.1	2.57
	4	9.14	0.59	43.5	2.35
$ZnO:PEIE_{10}$	0.3	8.97	0.57	51.6	2.64
	1	9.02	0.58	48.4	2.53
	2	8.83	0.57	47.2	2.38
	4	8.63	0.57	45.1	2.22

TABLE II
PERFORMANCE OF SPRAY-COATED 1 × 8 cm^2 OPVS WITH AND WITHOUT AN INKJET-PRINTED Ag GRID ON AN ITO GLASS CATHODE

Pitch size (cm)	J_{sc} (mA cm^{-2})	V_{oc} (V)	FF	PCE (%)	PCE* (%)
w/o grid	9.42	0.52	39.0	1.91	1.91
4	9.47	0.54	42.3	2.16	2.22
2	9.19	0.55	48.8	2.47	2.60
1	8.88	0.55	50.2	2.45	2.70

*PCE corrected for shadow effect.

increasing strip length were observed for both OPVs with different ETLs. The variations in the open-circuit voltage (V_{oc}) and J_{sc} are not sensitive to increases in the strip length. These factors indicate that the performance is substantially affected by the transverse charge transport along the strip length within the bulk active layer and ETL. These transverse paths are also coupled to some defects or traps (in them) hindering charge transport in the vertical and strip width directions. These defects or traps might be caused by the inhomogeneity or quality of the large-area coating. Because such defects block charge transport, an enforced 3-D charge transport network (especially in the transverse direction) within the OPV is necessary to mitigate the decrease or loss of PCE caused by these coating defects. By the PEIE modification, the PCE loss can be reduced to ~15% when the device area is increased from 1 × 0.3 to 1 × 4 cm^2. However, when we further increased the device area to 1 × 8 cm^2, the PCE and FF still dramatically dropped to 1.9% and 39%, respectively, as shown in Table II. The PCE of the large-area devices (8 cm^2) is still only ~70% of that of the reference devices (0.3 cm^2). This

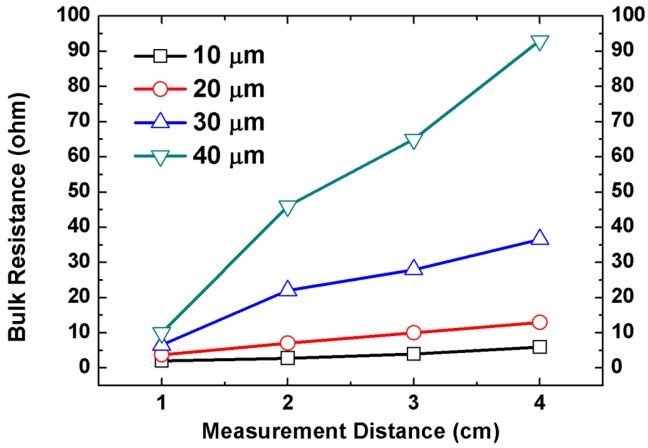

Fig. 3. Bulk resistance of silver grids printed at different drop spacing at different measurement distances from 1 to 4 cm.

implies that the ETL modification is not enough to fully resolve the issue of PCE reduction. Therefore, we propose the introduction of a set of simple and low-cost grid lines easily printed on the ITO substrate to solve this problem.

B. Inkjet Printed Silver Grids as an Auxiliary Electrode for Large-Area Organic Photovoltaics

This design of the grid can enforce transverse charge transportation as a path to bypass any local hindrance in the vertical and width directions and also solve the issue of increased impedance due to the extension of transverse area. Prior to the design test, the thickness and width of grid were considered, as they are closely related to the resistance of the line itself. In this study, we deposited IJP Ag grids to improve the transverse charge transport in the large-area sprayed OPVs, and the resistance of the Ag grids is greatly influenced by the drop spacing of the silver ink. Our previous study demonstrated that a continuous IJP Ag grid can be formed if the drop spacing is smaller than 40 μm [15]. However, the effect of drop spacing on the conductivity of Ag grids is seldom investigated. Therefore, the effect of drop spacing on the conductivity of the Ag grids was first studied. We inkjet printed various Ag grids at different drop spacings including 10, 20, 30, and 40 μm, and measured the bulk resistance with different measurement distances from 1 to 4 cm. Fig. 3 shows that the Ag grids deposited with drop spacings of 10 and 20 μm still exhibited a low bulk resistance as the measurement distance was extended to 4 cm. As the drop spacing was raised to 30 and 40 μm, the increasing bulk resistance of the Ag grids with long measurement distance implies that the printed Ag grids cannot be conductive enough for long-distance charge transport. In addition, the increase in the Ag grid width could enhance the grid conductivity as well as the shadow effect on the OPVs. An increase in the grid thickness (determined by the drop spacing of inkjet printing) could not only enhance the grid conductivity but also increase the cost and time of printing. Considering the above factors and the optimal performance of OPVs, we inkjet printed the Ag grids with a drop spacing of 10 μm for the auxiliary electrode and set the thickness and

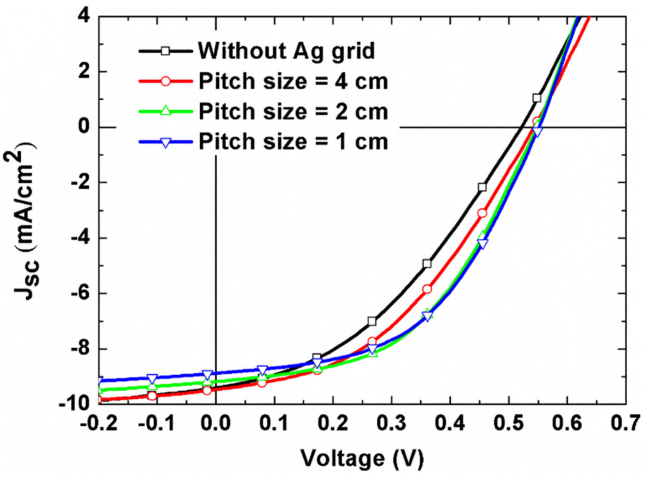

Fig. 4. Current–voltage curves of spray-coated 1×8 cm^2 OPVs without and with Ag grids of different pitch sizes based on ZnO/PEIE ETL and ITO glass.

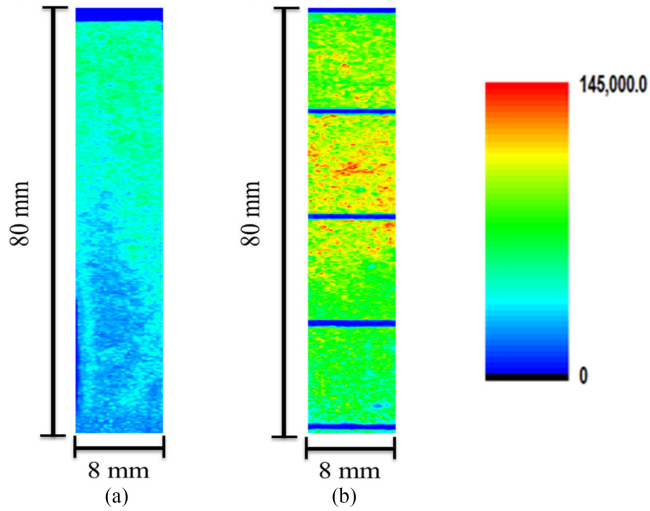

Fig. 5. Two-dimensional current (EQE) mapping measured by LBIC for the 1×8 cm^2 OPVs (a) without and (b) with a Ag grid. The relative current density is scaled by the color bar. Red color represents high current density.

width of the inkjet-printed Ag grids to ∼500 nm and 1 mm, respectively. This is different from our previous ITO-free design of printed Ag grids with a thickness and width of ∼200 nm and 0.2 mm, respectively, where transparency and sheet resistance were the primary concerns [15], [21].

The other important factor for Ag grids as the auxiliary electrode is the separation distance between grid lines, which is defined as the pitch size (see Fig. 1). Three patterns of Ag grids with pitch sizes of 1, 2, and 4 cm were adopted to prepare spray-coated 1×8 cm^2 OPVs based on ZnO/PEIE ETL and ITO glass. The current–voltage curves of the corresponding OPVs are shown in Fig. 4, and the performance of these OPVs and the reference OPV (without Ag grid) are compared in Table II. As compared to the abovementioned 4 cm^2 device, the PCE of the reference device (8 cm^2) decreased to 1.91%. This PCE reduction is mainly a result of the low fill factor due to the long charge transport path. For the devices with Ag grids with a pitch size of 4 cm, the PCE and fill factor increased to 2.2% and 42.3%, respectively, compared to those of the reference OPV without an Ag grid (1.9% and 39.0%). When the pitch size was increased to 2 and 1 cm, the fill factor was enhanced to 48.8% and 50.2%, respectively. This indicates that the overall transport and loss/recombination of charge carriers are improved by shortening the transverse transport length. However, the corresponding PCE values were 2.5% for both OPVs. It is obvious that the shortest pitch size (1 cm; high density of IJP Ag grids) results in a significant shadow effect on the OPV and thus reduces the PCE. After correcting for the shadow effect for the OPV with pitch size of 1 cm (7 sliver grids in the devices), the corresponding PCE would be 2.7% (modified active layer area is 7.3 cm^2), which is the same as that of the smaller OPVs with a device area of 1×1 or 1×0.3 cm^2. This also suggests that there is almost no transport loss in any direction within the 1×1 cm^2 device, although coating defects and inhomogeneities can still exist in the device. To optimize the PCE while minimizing the shadow effect and Ag cost, a pitch size of 2 cm is the best choice. Corresponding to the spray-coated 1×1 cm^2 OPV (PCE = 2.80%), this design can reduce the PCE loss of the spray-coated 1×8 cm^2 OPV to 11% compared with that (= 32%) for the same size of OPV without an Ag grid. The simple design concept proposed here can be easily integrated into an OPV module.

To clarify the effect of IJP Ag grids on the charge transport, Fig. 5 shows the 2-D mapping of the current distribution as measured by the LBIC technique for the 1×8 cm^2 OPVs without and with Ag grids. The coating inhomogeneity (film thickness variation, local defects, etc.) can be visibly examined by the LBIC technique [22]. The current mapping of the OPV without an Ag grid [see Fig. 5(a)] has a low average intensity and a large region of inhomogeneity or defect distribution (green color). In contrast, Fig. 5(b) shows that a uniform and thin region in the film can produce high current (red color). Areas shadowed by the grid lines can be seen to have the lowest intensity (blue color). Both OPVs were fabricated with the same process except for the adoption of the ITO-coated glass with and without an IJP Ag grid. The representative mappings are shown in Fig. 5. Obviously, the patterned Ag grid lines enhance the transport of charge carriers in the length (transverse) and width directions. Therefore, it can be deduced that an Ag grid can form conducting paths that bypass local inhomogeneities or defect regions. It seems that the local regions of inhomogeneities and defects can be partly activated. This study proposes that a simple patterned Ag grid can greatly reduce the degradation effect caused by the large-area coating process.

IV. Conclusion

We demonstrated a simple method to improve the performance of large-area spray-coated OPVs by embedding inkjet-printed Ag grids into the ITO substrate. First, we modified the ETL with PEIE to decrease the PCE reduction from ∼30% to ∼15% when the device area was increased from 0.3 to 4 cm^2. The improved large-area performance was obtained because of

the reduction in the surface defects of the ETL. Moreover, we introduced an Ag grid onto the ITO substrate to improve charge carrier transport in the transverse direction. A PCE of ∼2.5% was achieved by an OPV with a device area of 8 cm^2 by tuning the Ag grid spacing. Our work shows a feasible method of fabricating high-performance sprayed large-area OPVs.

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